UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/665,880	09/19/2003	Alexander Gidon	CAD 362	6774

22862   7590   12/21/2007

GLENN PATENT GROUP
3475 EDISON WAY, SUITE L
MENLO PARK, CA 94025

EXAMINER
DINH, PAUL

ART UNIT	PAPER NUMBER
2825	

MAIL DATE	DELIVERY MODE
12/21/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

	Application No.	Applicant(s)
Office Action Summary	10/665,880	GIDON ET AL.
	Examiner	Art Unit	
	Paul Dinh	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>07 November 2007</u>.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>4-12</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>4-12</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on <u>11 February 2004</u> is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date <u>4/6/06</u>.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____ .

DETAILED ACTION

This is a response to the election filed on 11/7/07.

Claims 4-12 are pending.

Specification

Brief description of the drawings need to indicate "prior art" to prior art drawings. Correction is required.

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Claims 5, 10-11 recite "buffers" and "buffer trees"; therefore, these features must be clearly shown/labeled in the drawings or these features canceled from the claim.

NO NEW MATTER SHOULD BE ENTERED.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:
The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

Claims 4-12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 4, 5, 10-11 are rejected because "standard" in "standard HDL" in claim 4, "typical" in "typical flip-flop delay" and 'typical load (capacitance)" in claims 5, 10, 11 are unclear as to what standard and what is considered typical. If "standard" and "typical" are the feature that the Applicant relies on, then "standard" and "typical" must be defined in the claims.

Claim 6 is rejected because "clocks all having a period of substantially zero" is unclear as to how a clock (or clocks) can have a period of substantially zero.

Claims 6-7 are rejected because "cycles" are unclear as to what cycles the Applicant is referring to.

Claim 8 is rejected because "slack equivalent" is unclear and incomplete, i.e., equivalent

between what.

Claim 9 is rejected because "the actual value" lacks antecedent basis.

Claim 12 is rejected because it is not clear what is meant by "zero-clocked cycle-breaking

flip-flops", 'applying a retiming algorithm" is unclear and incomplete as to applying a retiming

algorithm to what, and "said retimed design" lacks antecedent basis.

Although the claims are interpreted in light of the specification, limitations from the

specification are not read into the claims. See In re Van Geuns, 988 F.2d 1181, 26

USPQ2d 1057 (Fed. Cir. 1993).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form
The basis for the rejections under this section made in this Office action:
A person shall be entitled to a patent unless –
(e) The invention was described in (1) an application for patent, published under section 122(b), by another filed in
the United States before the invention by the applicant for patent or (2) a patent granted on an application for
patent by another filed in the United States before the invention by the applicant for patent, except that an
international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this
subsection of an application filed in the United States only if the international application designated the United
States and was published under Article 21(2) of such treaty in the English language.

Claims 4-10, 12 are rejected under 35 U.S.C. 102(e) as being anticipated by the prior art

of record Oktem (US pub. 20070174794)

(Claim 4) describing a digital circuit using a standard HDL (par 0003-0004);

Constructing said digital circuit from said HDL description (par 0003-0004); and

Replacing flip-flops in said digital circuit with negative delay elements (fig 18-20, 24).

(Claims 5-10, 12) wherein said negative-time elements are implemented by buffers

having a delay -T, where T is a delay equal to a flip-flop's clock period less a typical flip-flop

delay (fig 18-20, 24); wherein if said digital circuit contains cycles, then performing the step of

breaking said cycles by inserting flip-flops clocked by clocks all having a period of

substantially zero delay (fig 18-20, 24); wherein cycles are only broken on backward paths (fig

27-29); wherein clocks and registers constructed have the property of slack equivalence,

wherein optimization goals at each gate are substantially the same as they would be if registers

were already optimally distributed (fig 18-25); wherein the actual value of T is set to a clock period of a flip-flop being replaced (fig 18-20, 31-35); using a buffer to replace a flip-flop, said buffer having a typical load capacitance, representing an average or weighted-average load capacitance taken over inputs of all gates and flip-flop D pins in a target technology library (fig 18-26); after logic optimization, reinstalling registers in place of negative-delay elements (fig 18-20, 24); removing all zero-clocked cycle-breaking flip-flops (par 0070, 0084, 0087, 0092, 0110); applying a retiming Algorithm (par 0083-0084, 0087-0088, 0092); and after retiming, performing a second logic optimization pass to fine-tune said retimed design (par 0083-0084, 0087-0088, 0092)

Claims 4-10, 12 are rejected under 35 U.S.C. 102(e) as being anticipated by the prior art of record Suaris (US pub. 20050132316)

(Claim 4) describing a digital circuit using a standard HDL (par 0003, 0077);

Constructing said digital circuit from said HDL description (par 0003, 0077); and

Replacing flip-flops in said digital circuit with negative delay elements (i.e., fig 5-7, 12-20).

(Claims 5-10, 12) wherein said negative-time elements are implemented by buffers having a delay -T, where T is a delay equal to a flip-flop's clock period less a typical flip-flop delay (fig 1-3, 12, 14, 15); wherein if said digital circuit contains cycles, then performing the step of breaking said cycles by inserting flip-flops clocked by clocks all having a period of substantially zero delay (i.e., one or more of: par 0047 0056-57, 0077-0079, 0081-0084); wherein cycles are only broken on backward paths (fig 7, 15, 18-20); wherein clocks and registers constructed have the property of slack equivalence (fig 14), wherein optimization goals at each gate are substantially the same as they would be if registers were already optimally distributed (i.e., one or more of: fig 4, 7, 13-17, 19-20); wherein the actual value of T is set to a clock period of a flip-flop being replaced (par 0005, 0043, 0055); using a buffer to replace a flip-flop, said buffer having a typical load capacitance, representing an average or weighted-average load capacitance taken over inputs of all gates and flip-flop D pins in a target technology library (fig 12-17); after logic optimization, reinstalling registers in place of

negative-delay elements (fig 12-17, 19-20); removing all zero-clocked cycle-breaking flip-flops (par 0084); applying a retiming Algorithm (fig 7, 9-15, 18); and after retiming, performing a second logic optimization pass to fine-tune said retimed design (fig 7, 9-15, 18)

Allowable Subject Matter

Claim 11 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul Dinh whose telephone number is 571-272-1890. If attempts to reach the examiner by telephone are unsuccessful, the examiner's Supervisor, Jack Chiang can be reached on 571-272-7483. The fax number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Paul Dinh
Primary Examiner